ABSTRACT OF THE DISCLOSURE

A frequency divider divides the external clock signal by two and generates a first clock signal for an even-numbered data patch and a second clock signal for an odd-numbered data, wherein the first clock signal is opposite in phase to the second clock signal. A column selection line enable control circuit generates even-numbered column selection line enable signals in response to the first clock signal and generates odd-numbered column selection line enable signals in response to the second clock signal. A switching circuit connects a pair of bit lines to a pair of even-numbered input/output (I/O) lines in response to the even-numbered column selection line enable signals and connects the pair of bit lines to a pair of odd-numbered I/O lines in response to the odd-numbered column selection line enable signals. An I/O line sense amplification circuit senses and amplifies even-numbered read data from the pair of even-numbered I/O lines and outputs the amplified even-numbered read data to a pair of data lines in response to the first clock signal, and senses and amplifies odd-numbered read data from the pair of odd-numbered I/O lines and outputs the odd-numbered read data to the pair of data lines in response to the second clock signal.